WHAT WE CLAIM ARE:

1. A semiconductor device comprising:

an underlie having a conductive region in a surface layer of said underlie;

an insulating etch stopper film covering a surface of said underlie;

an interlayer insulating film formed on said insulating etch stopper film;

a wiring trench formed in said interlayer insulating film, said wiring trench having a first depth from a surface of said interlayer insulating film;

a contact hole extending from a bottom surface of said wiring trench to a surface of the conductive region through a remaining thickness of said interlayer insulating film and through said insulating etch stopper film; and

a dual damascene wiring layer embedded in said wiring trench and in said contact hole,

wherein said interlayer insulating film includes a first kind of an insulating layer surrounding a side wall and the bottom surface of said wiring trench and a second kind of an insulating layer disposed under the first kind of the insulating layer and having etching characteristics different from the first kind of the insulating layer.

2. A semiconductor device according to claim 1, wherein said contact hole has a portion whose cross sectional area gradually increases toward an upper level in the first kind of the insulating layer.

3. A semiconductor device according to claim 1, wherein said interlayer insulating film further includes a third kind of an insulating layer under the second kind of the insulating layer, the third kind of the insulating layer having etching characteristics different from the second kind of the insulating layer.

4. A semiconductor device according to claim 3, wherein said contact hole has a portion whose cross sectional area gradually increases from an intermediate level of the second kind of the insulating layer toward an upper level.

5. A semiconductor device according to claim 3, wherein the second kind of the insulating layer is capable of functioning as an etch stopper while the first kind of the insulating layer is etched, and said contact hole has a substantially same cross sectional shape from a bottom surface of the second kind of the insulating layer to the surface of the conductive region.

6. A semiconductor device according to claim 3, wherein the third kind of the insulating layer has a thickness thinner than the first depth.

7. A semiconductor device according to claim 1, wherein the second kind of the insulating layer is disposed on said insulating etch stopper film and has a thickness thinner than the first depth.

8. A method of manufacturing a semiconductor device, comprising the steps of:

forming an insulating etch stopper film on an underlie having a conductive region in a surface layer of the underlie;

forming an interlayer insulating film on the insulating etch stopper film, the interlayer insulating film including a first kind of an insulating layer and a second kind of an insulating layer formed under the first kind of the insulating layer, the second kind of the insulating layer having etching characteristics different from the first kind of the insulating layer;

forming a first contact hole extending from a surface of the interlayer insulating film to the insulating etch stopper film through the interlayer insulating film;

embedding an organic protective filler in the contact hole to a height lower than a surface of the second kind of the insulating layer;

forming a wiring trench in the first kind of the insulating layer of the interlayer insulating film, the wiring trench having a first depth from the surface of the interlayer insulating film and overlapping or including the first contact hole as viewed in plan;

removing the protective filler;

removing the insulating etching stopper film exposed in the first contact hole to form a second contact hole continuous with the first contact hole and reaching the underlie having the conductive region; and

forming a dual damascene wiring layer embedded in the wiring trench and the first and second contact holes.

9. A method of manufacturing a semiconductor device according to claim 8, wherein the interlayer insulating film further includes a third kind of an insulating layer disposed under the second kind of the insulating layer, the third kind of the insulating layer having etching characteristics different from the second kind of the insulating layer.

10. A method of manufacturing a semiconductor device according to claim 9, wherein the second kind of the insulating layer has an etch rate lower than etch rates of the first and third kinds of the insulating layers.

11. A method of manufacturing a semiconductor device according to claim 8, wherein the second kind of the insulating layer includes another etch stopper layer and an

underlying insulating film disposed under said another etch stopper layer, and said step of forming the first contact hole forms the first contact hole reaching the etch stopper film passing through the first kind of the insulating layer and the second kind of the insulating layer including said another etch stopper layer and the underlying insulating film.

12. A method of manufacturing a semiconductor device, comprising:

a step of forming an insulating etch stopper film on an underlie having a conductive region in a surface layer of the underlie;

a step of forming an interlayer insulating film on the insulating etch stopper film, the interlayer insulating film including a first kind of an insulating layer and a second kind of an insulating layer formed under the first kind of the insulating film, the second kind of the insulating layer having etching characteristics different from the first kind of the insulating layer;

a first etching step of forming a first contact hole extending from a surface of the interlayer insulating film to the second kind of the insulating layer through the first kind of the insulating layer by etching;

a second etching step of forming a wiring trench in the first kind of the insulating layer of the interlayer insulating film and removing a remaining interlayer insulating film under the first contact hole by etching, the wiring trench having a first depth from a surface of the interlayer insulating film and overlapping or including the first contact hole as viewed in plan;

a step of removing the insulating etch stopper film exposed in the first contact hole to form a second contact hole continuous with the first contact hole and reaching the underlie having the conductive region; and

a step of forming a dual damascene wiring layer embedded in the wiring

trench and in the first and second contact holes.

13. A method of manufacturing a semiconductor device according to claim 12, wherein said second etching step includes a step of etching the second kind of the insulating layer to expose the etch stopper film and a step of partially etching the exposed etch stopper film.

14. A method of manufacturing a semiconductor device according to claim 12, wherein the second kind of the insulating layer includes another etch stopper film and an underlying insulating film formed under said another etch stopper film, said first etching step includes a step of etching the first kind of the insulating layer by using a mask and a step of etching the exposed another etch stopper film, and said second etching step includes a step of etching the underlying insulating film under the first contact hole and a step of partially etching the exposed etch stopper film.

15. A method of manufacturing a semiconductor device according to claim 12, further composing the step of forming a hard mask layer on the interlayer insulating film, wherein said first etching step includes a step of forming a first resist mask on the hard mask layer, and said second etching step includes a step of forming a second resist mask on the hard mask layer and etching the hard mask layer and a step of removing thereafter the second resist mask and etching the interlayer insulating film by using the hard mask layer as an etching mask.

16. A method of manufacturing a semiconductor device, comprising:

a step of forming an insulating etch stopper film on an underlie having a conductive region in a surface layer of the underlie;

a step of forming an interlayer insulating film on the insulating etch stopper film, the interlayer insulating film including first, second and third kinds of insulating layers formed in this order from a bottom, the second kind of the insulating layer having etching characteristics different from the first and third kinds of the insulating layers;

a first etching step of forming a contact hole extending from a surface of the interlayer insulating film to the insulating etch stopper film through the third, second and first kinds of the insulating layers by etching;

a step of disposing an organic protective filler in the contact hole, the filler being higher than a surface of the first kind of the insulating layer and lower than a surface of the second kind of the insulating layer;

a second etching step of forming a wiring trench in the third kind of the insulating layer of the interlayer insulating film by etching, the wiring trench having a first depth from a surface of the interlayer insulating film and overlapping or including the contact hole as viewed in plan;

a step of removing the protective filler to expose the insulating etch stopper film in the contact hole;

a third etching step of etching the exposed etch stopper film; and

a step of forming a dual damascene wiring layer embedded in the wiring trench and in the contact hole.

17. A method of manufacturing a semiconductor device, comprising:

a step of forming an insulating etch stopper film on an underlie having a conductive region in a surface layer of the underlie;

a step of forming an interlayer insulating film on the insulating etch stopper film, the interlayer insulating film including first, second and third kinds of

insulating layers formed in this order from a bottom, the second kind of the insulating layer having etching characteristics different from the first and third kinds of the insulating layers;

a first etching step of forming a contact hole extending from a surface of the interlayer insulating film to the second kind of the insulating layer through the third kind of the insulating layer by etching;

a second etching step of etching the second kind of the insulating layer exposed at a bottom of the contact hole;

a third etching step of forming a wiring trench in the third kind of the insulating layer of the interlayer insulating film and simultaneously etching the first kind of the insulating layer under the contact hole to expose the etch stopper film, the wiring trench having a first depth from a surface of the interlayer insulating film and overlapping or including the contact hole as viewed in plan;

a fourth etching step of etching the exposed etch stopper film; and

a step of forming a dual damascene wiring layer embedded in the wiring trench and the contact hole.

18. A method of manufacturing a semiconductor device according to claim 17, further comprising the step of forming a hard mask layer on the interlayer insulating film, wherein said first etching step includes a step of forming a first resist mask on the hard mask layer and a step of etching the hard mask layer by using the first resist mask as an etching mask, and said third etching step includes a step of forming a second resist mask on the hard mask layer and etching the hard mask layer by using the second resist mask as an etching mask and a step of removing thereafter the second resist mask and etching the interlayer insulating film by using the hard mask layer as an etching mask.